

**REMARKS**

As a preliminary matter, the drawings (Fig. 3) are objected to based on the reasons set forth of page 2 of the present Office Action. Applicants submit herewith a corrected Fig. 3, to correct the misspelling of “INFORMATION.”

Claims 1-25 are all the claims pending in the present application, new claim 25 having been added as indicated herein. Applicants thank the Examiner for indicating that claims 3-10, 15, and 16 are allowed, and that claims 11-14, 17, and 20-24 are indicated as containing allowable subject matter. Claims 11-14, 17 and 20-24 would be allowable if rewritten in independent form including all of the limitations of the based claim and any intervening claims. Claims 1, 2, 18, and 19 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Walley et al. (US Patent No. 6,421,283).

With respect to independent claim 1, Applicants previously argued that Walley does not disclose or suggest at least, “replacing defective cells in the memory with spare memory provided in the memory controller when there is a request for access to the defective cells of the memory,” as recited in claim 1 (emphasis added). In response to this argument, the Examiner maintains the same arguments set forth in the previous Office Action and cites a few new elements and column/line numbers in Walley. Based on Applicant’s initial understanding of the Examiner’s arguments, it appeared that the Examiner believed that T&P logic circuit 308 corresponds to the claimed memory controller. However, the Examiner clarified that he has grouped T&P logic circuit 308 along with RAM 309 to allegedly satisfy the claimed memory controller.

Applicants amend independent claim 1 and submit that Walley does not disclose or suggest the limitation set forth in the previous paragraph and does not disclose or suggest at least, “wherein the memory controller and the memory are separate elements.” That is, since Walley shows that the RAM 309 is clearly coupled with RAM 306 (which appears to correspond to the claimed memory and is separate from the T&P logic circuit) (*see Fig. 3 of Walley*), Walley clearly does not satisfy the features of the memory controller and memory being separate elements and “replacing defective cells in the memory with spare memory provided in the memory controller when there is a request for access to the defective cells of the memory,” as the RAM 309 (i.e., alleged spare memory) of Walley can not be provided in the memory controller if the RAM 309 is coupled with the RAM 306 (i.e., alleged ‘memory’).

Further, if the Examiner maintains the position that the T&P logic circuit 308 and RAM 309, together, satisfy the feature of replacing defective cells in the memory with spare memory provided in the memory controller, then clearly the feature of the memory controller and the memory being separate elements cannot be satisfied, as the RAM 309 is coupled to the RAM 306, and the RAM 306 of Walley is separate from the T&P logic circuit 308 (i.e., alleged memory controller).

In other words, the two-quoted features of claim 1 discussed above can not be mutually satisfied by Walley. Therefore, since all of the limitations of claim 1 are not satisfied by Walley, Applicants maintain that Walley does not anticipate claim 1.

Therefore, at least based on the foregoing, Applicants maintain that Walley clearly does not anticipate claim 1.

Applicants submit that independent, amended claim 18 is patentable at least based on reasons similar to those set forth above with respect to independent claim 1.

Applicants amend claims 11, 12, 17, 18, 20, and 21, so that claims 11-14, 17, and 20-24 are not affected by the amendments to independent claims 1 and 18.

Applicants submit that dependent claims 2 and 19 are patentable at least by virtue of their respective dependencies from independent claims 1 and 18.

Also, Applicants add new claim 25 to provide a varying scope of coverage. Applicants submit that the prior art does not disclose or suggest at least, “replacing defective cells in the memory with spare memory provided in the memory controller when there is a request for access to the defective cells of the memory,” and “wherein said spare memory is not coupled with said memory.”

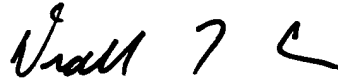
In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Amendment Under 37 C.F.R. § 1.111  
U.S. Appln. No. 10/612,300

Attorney Docket No. Q75923

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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WASHINGTON OFFICE

**23373**

CUSTOMER NUMBER

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**AMENDMENTS TO THE DRAWINGS**

Applicants submit herewith a corrected Fig. 3, to correct the misspelling of  
“INFORMATION.”

Attachment: Formal Drawing  
Replacement Sheet